REMARKS

Claims 1-10 remain pending in this application with claims 1 and 8 being amended by this response.

Rejection of claims 1, 8 and 10 under 35 U.S.C. 112, second paragraph

Claim 1, 8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as having insufficient antecedent basis for all terms contained therein. Claims 1 and 8 have been amended in accordance with the comments in the Office Action to provide antecedent basis for all terms. In view of the amendments to the claims, it is respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of claims 1-8 and 10 under 35 U.S.C. 103(a)

Claims 1-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Demura (U.S. Publication No. 2002/0099996) in view of Greenblat (U.S. Publication No. 2003/0212830) and further in view of Yuan (U.S. Patent No. 6,526,477).

The present arrangement as claimed in claim 1 provides a method for error correction of an encoded data stream. The method includes saving a demodulated data stream in an input buffer and performing a first correction process on-the-fly in the input buffer. After correction, the data is transferred to an external DRAM. The data is copied from the external DRAM to an embedded SRAM and a multipass correction is started in the embedded SRAM. The corrected data is copied back from the embedded SRAM to the external DRAM after multipass correction. Claim 8 is directed to an apparatus for error correction of an encoded data stream and includes features similar to those discussed above regarding claim 1. Thus, all arguments presented hereinbelow apply to both claims 1 and 8.

The present claimed method and apparatus allows for the correction process to be performed in the fast internal SRAM while the input/output streaming is performed in by a comparatively slow external DRAM. In this way, the number of random accesses to the external DRAM is reduced. After gathering a full ECC block in the DRAM, the data is streamed to the embedded internal SRAM where the ECC block is corrected via multipass correction, and streamed back to the DRAM. The size of the internal SRAM is reduced. The internal SRAM correction simplifies the hardware complexity during the correction process and the overall correction process is sped up (see Specification page 2, lines 17-32). These features are neither disclosed nor suggested by the prior art.

Demura describes a method for detecting and correcting errors and erasures in product ECC-coded data arrays for DVD systems. The received data blocks are stored in a main DRAM memory 12. Part of the received data blocks are copied from the main DRAM memory (12) to a buffer SRAM memory (13) to calculate correction bit patterns (paragraph 55). The buffer memory includes sections (14, 15) for storing rows and columns of the data blocks and additional sections (14A, 15A) for storing dense maps identifying the error locations and correction bit patterns. The correction is effectuated as indexed by the dense map (paragraph 13). Neither buffer memory sections 14, 15 nor 14A, 15A include the corrected data blocks at any method step. The data are not corrected in the SRAM, but in the DRAM based on the dense maps stored in the SRAM (Fig. 6 step 49, paragraph 55). Subsequently, the erroneous data is identified, the address of the erroneous data in the main memory 12 is calculated and the erroneous data is corrected using the correction bit pattern and stored in the main memory 12, as described in paragraph 55. Thus, Demura neither discloses nor suggests "performing a first correction process on-the-fly in the input buffer" as recited in the present claimed arrangement. As data is not corrected in the SRAM, Demura also cannot disclose or suggest "starting a multipass correction in the embedded SRAM" as recited in the present claimed arrangement.

Greenblat describes a system for implementing a ring architecture for communications and data handling systems and the enumeration process for

automatically configuring the ring topology. Means for copying data frames from an external DRAM to an embedded SRAM are shown within this context. Greenblat was cited to show copying of a data from the external DRAM to an embedded SRAM and back. However, a data correction process as claimed in claim 1 of the present application is not shown in Greenblat. Specifically, Greenblat, similarly to Demura, neither discloses nor suggests "performing a first correction process on-the-fly in the input buffer" as recited in the present claimed arrangement. Greenblat, similarly to Demura, also neither discloses nor suggests "starting a multipass correction in the embedded SRAM" as recited in the present claimed arrangement.

Yuan describes a host-memory based Redundant Array of Independent Disk (RAID) system, the host computer having a host memory for storing data and parity data and having a RAID controller for interfacing disk drives with the host computer. The RAID controller receives new data from the host memory for storage and is configured to generate new parity data by performing one or more XOR operations.

Yuan was cited to show an input buffer for performing a correction process on-the-fly. However, Column 8, lines 42-52 cited in the Office Action, show an XOR operation using the new data and the old data. The result of this XOR operation and the old parity data are used as inputs for an ensuing XOR operation. Therefore, the cited text basically shows an XOR operation "to generate final XOR result of old parity data, new (parity) data and old data" which is the new parity data. It is assumed from the description of the cited passage that by "new parity data" in column 8, line 50 in fact new data is meant. Therefore, Yuan describes how to generate new parity data from old parity data, new data and old data. This is different from the correction process claimed in independent claim 1 of the present application where parity data is used to correct the read out data in case of bit errors. Furthermore, in Yuan, the new parity data is then written to the XOR buffer 222 in the host memory for storage, that is to say, the results are written to a buffer different from the buffers in which the input signals are stored. In claim 1 of the present application, the correction process is performed on-the-fly in the input buffer, that is to say, the result of the correction process is available in the input buffer, not in a different buffer. Thus, Yuan (with Demura and Greenblat) neither

discloses nor suggests "performing a first correction process on-the-fly in the input buffer" as recited in the present claimed arrangement. Yuan, similarly to Demura and Greenblat, also neither discloses nor suggests "starting a multipass correction in the embedded SRAM" as recited in the present claimed arrangement.

It is respectfully submitted that none of the cited references disclose or suggest correcting erroneous data blocks on-the-fly in the fast SRAM. Thus, a combination of Demura, Greenblat and Yuan, also neither disclose nor suggest "performing a first correction process on-the-fly in the input buffer" as recited in the present claimed arrangement. The cited references to Demura, Greenblat and Yuan also neither discloses nor suggests "starting a multipass correction in the embedded SRAM" as recited in the present claimed arrangement. Thus, any combination of these references also cannot disclose or suggest this feature.

In view of the above remarks, it is respectfully submitted that claims 1 and 8 are patentable over Demura, Greenblat and Yuan when taken alone or in any combination. As claims 2-7 and 10 are dependent on claim 1, it is respectfully submitted that these claims are allowable for the same reasons as claim 1. Thus, it is further respectfully submitted that this rejection is satisfied and should be withdrawn.

Claim 9 has been indicated as allowable if rewritten in independent form including the features of the base and any intervening claim. In view of the above remarks, it is respectfully submitted that claims 1 and 8 are allowable in their present form and thus claims 2-7, 9 and 10 are also allowable in view of their dependence on claims 1 and 8.

Having fully addressed the Examiner's rejections, it is believed that, in view of the amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due with this response. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,
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